cap-XX

Compact Flash™ Extender and Supercapacitor Evaluation Board

Part No. APPEB1004

User's Manual

Revision 1.0 March, 2003

Evaluation Board Features

- CF Extender
- Supercapacitor (two form factors)
- Adjustable current limit circuit with Supercapacitor charge enable
- 3.3V and 5V input LEDs
- Supercapacitor voltage comparator with adjustable threshold, adjustable hysteresis and Power Good LED
- Card Detect switches to simulate card removal and insertion
- Sub-circuits can be disconnected to reduce the load
- Test points, jumpers and I/O connectors

Typical Supercapacitor Applications

- Compact Flash
- PC card
- PDA
- Smartphone
- GPRS
- Handheld Equipment
- Load Leveling

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1.0 Introduction

This User's Manual is for the cap-XX Compact Flash[™] (CF) Extender and Supercapacitor Evaluation Board (Part No. APPEB1004). This board was designed for the evaluation of a supercapacitor in a CF Card. The application of supercapacitors is limited only by the user's imagination. Typical examples are CF, PC Card, PDA, Smartphone, GPRS and other handheld equipment.

The Evaluation Board is a CF Extender with a supercapacitor, a current limit circuit and other features.

An excellent source for information on Supercapacitors and free downloads are available on the cap-XX website at <u>www.cap-xx.com</u>.

In the following description of operation it may be helpful to refer to the Evaluation Board Schematic in the Appendix.

2.0 Input Voltage

The supercapacitors for the Evaluation Board are rated at 4.5V and therefore it is not recommended that the input voltage (V_{CC}) be greater than 4.5V. If V_{CC} is 5V then the Equivalent Series Resistance (ESR) rise rate of the supercapacitor is increased and the lifetime will be reduced. A red LED is included to indicate that V_{CC} is too high and it starts to glow when V_{CC} is approximately 4.2V. The red LED is labeled on the Evaluation Board as "5 Volts". If V_{CC} is 5V then the voltage can be dropped to < 4.5V by removing a jumper which introduces a series diode in the voltage supply lines on the Evaluation Board (see section 7.0). A yellow LED is included to indicate when V_{CC} is 3.3V or greater. It is labeled on the Evaluation Board as "3.3 Volts".

If V_{CC} is disconnected (or if the Evaluation Board is removed from the host) and there is still charge on the supercapacitor then current will flow through the body diode of M1 and through the yellow LED (also through the red LED if the supercapacitor is greater than ~ 4.2V). The intensity of the yellow LED then gives an indication of the voltage remaining on the supercapacitor. If, however, the series diode has been included to reduce the 5V rail to 4.5V then the LEDs will not be ON when V_{CC} is disconnected.

2.1 Charge Time

A fully discharged supercapacitor will be charged to V_{CC} after a certain time (t_c). This time will depend on the current limit (I_L), V_{CC} and the capacitance (C). The equation is

$$t_{c} = \frac{CV_{CC}}{I_{L}}$$
(1)

3.0 Current Limit

Circuits that employ large capacitors generally need a current limiting circuit to alleviate the current in-rush problem. The CF specification states that the peak current is 500mA from either the 3.3V or 5V rail. The tolerance on the 3.3V rail is \pm 5% and the tolerance on the 5V rail is \pm 10%. Therefore the peak power from the 3.3V rail is 1.65W \pm 5% and the 5V rail is 2.5W \pm 10%.

The Evaluation Board has an adjustable current limit circuit. The current limit can be adjusted from 0A to \sim 4.5A by using the potentiometer R2. It is labeled on the Evaluation Board as "Current Limit". Turning the potentiometer clockwise will increase the current limit.

The MOSFET (M1) and Sense Resistor (R1) can withstand up to 4.5A whilst the supercapacitor is being charged. They cannot however withstand the 4.5A into a short circuit indefinitely. There is no short circuit protection. The MOSFET (M1) has a maximum continuous power dissipation of 2.5W. Therefore any continuous load resistance (R_L) has a minimum value as given by equation 2.

$$R_{L} \ge \frac{V_{CC}I_{L} - 2.5}{I_{L}^{2}} \qquad [V_{CC}I_{L} > 2.5]$$

$$R_{L} = 0 \qquad [V_{CC}I_{L} \le 2.5]$$
(2)

 R_L also has a minimum power rating according to equation 3.

$$P_{R_{L}} > I_{L}^{2}R_{L} \qquad [\text{input current} = I_{L}] \qquad (3)$$

$$P_{R_{L}} > \frac{V_{CC}^{2}}{R_{L}} \qquad [\text{input current} < I_{L}]$$

4.0 Enable

The current limit circuit has an enable feature. *Enable* is an active low signal and the two pin jumper is labeled on the Evaluation Board as "J_ENABLE". It is an input signal to the Evaluation Board and it can be jumpered to ground, to be permanently enabled, or it can be externally driven by an open collector or drain. When "J_ENABLE" is externally driven it allows the supercapacitor to be charged only when the User's Card is ready. Pin 2 of "J_ENABLE" is the control input and Pin 1 is permanently connected to ground.

5.0 Power Good

The Power Good circuit (PGOOD) is included to indicate when the supercapacitor is charged to the appropriate level. The voltage on the supercapacitor is compared to a reference using a comparator with adjustable thresholds and hysteresis. The thresholds need to be adjustable on an Evaluation Board because different applications will require different load voltages. The hysteresis also needs to be adjustable because a step in load current will cause a step voltage on the supercapacitor because of the supercapacitor's Equivalent Series Resistance (ESR).

Since this step voltage (part of the ripple) is a normal occurrence, it would not be desirable for this to indicate that the supercapacitor is undercharged.

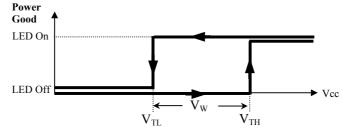


Figure 1 Power Good Hysteresis

As in Figure 1, the high threshold (V_{TH}) is the voltage at which the supercapacitor's unloaded voltage becomes acceptable. The hysteresis (V_W) is the voltage that when subtracted from the high threshold gives the low threshold (V_{TL}). It indicates that the supercapacitor is undercharged. V_{TH} is set by the factory at 3.2V and V_W is set at 0.3V, therefore V_{TL} is 2.9V.

PGOOD has a header labeled on the Evaluation Board as "H_PGOOD". It is an active high output signal that can be used to signal an external circuit that the supercapacitor is fully charged. A green LED is also included to indicate this condition. It is labeled on the Evaluation Board as "Power Good".

6.0 Adjusting the Circuit

Equipment needed: Adjustable power supply, multi-meter and various power resistors

Warning: Be careful not to exceed the supercapacitor rated voltage (4.5V) or the maximum continuous power rating for M1 (2.5W)

- (a) Ensure the following jumpers are fitted; "J_RED&YLW", "J_GREEN", "J_PGOOD", "J_ENABLE", "J_VCC13_IN" (pins 3 and 4), "J_VCC38_IN" (pins 3 and 4) and "J_5V". Remove jumpers on "J_VCC13_OUT" and "J_VCC38_OUT". Pin 1 is marked with "∇".
- (b) Turn "Current Limit" R2 fully anti-clockwise (no current). Set the power supply voltage to say 3.3VDC. Ensure that the power supply can supply the desired current. Connect its negative lead to J_GND1 or J_GND2. Connect the positive lead to pin 1 of "J_VCC13_IN".
- (c) Set the power supply output voltage to a value < 4.5V.

6.1 Adjusting the Current Limit with "Current Limit" - R_2 **Warning:** the maximum average power rating for M1 is 2.5W (see section 3.0)

(a) Connect a load resistor to "CON_CAPXX" (R_L) that draws just over the desired current limit from the CF host (typically 500mA). Note the power

rating of the resistor is according to equation 3 and R_L has a minimum value according to equation 2. For example, if the supply voltage is 3.3V and the desired current limit is 500mA then an R_L < 6.6 Ω would draw more than 500mA. R_L can then be chosen to be the next standard value < 6.6 Ω , ie 5.7 Ω . From equation 3, the power rating of the 5.7 Ω resistor would have to be > 1.43W. In this particular example, and according to equation 2, R_L can also be a short circuit as this would not overload M1.

(b) Place an ammeter in series with the power supply. Turn on the power supply and adjust "Current Limit" - R2 slowly clockwise until the desired current limit is reached.

Warning: Do not increase the current limit above that used in equations 2 and 3 for any longer than a few seconds otherwise M1 or R_L may be destroyed.

(c) Remove R_L , turn off the power supply.

6.2 Adjusting Hysteresis Width with "PGOOD Feedback" - R_{23} **NOTE:** V_W is adjusted before V_{TH} because the V_{TH} adjustment is affected by V_W . Therefore if adjustments are made in this section then section 6.3 should be checked.

- (a) If the CF card is to be driven from the 5V rail, then remove the jumper across "J_5V", otherwise, if the PC Card is to be driven from the 3.3V rail, then fit the jumper across "J_5V".
- (b) Connect a load power resistor (R_L) of around 10Ω -47 Ω from "VCC_OUT" to "GND_OUT" on "CON_CAPXX". This ensures that the supercapacitor voltage will change in reasonable time when the power supply voltage is changed. Note the power rating of R_L has to be a minimum value according to equation 3.
- (c) Turn the "PGOOD Reference" R_{15} to around mid position (about 11 turns from either limit).
- (d) Decide the high threshold voltage V_{TH} , the low threshold voltage V_{TL} and the hysteresis voltage width V_W (V_w = V_{TH} V_{TL}). V_{TL} has to be greater than the minimum voltage required by the Pulsed Load. V_W has to be greater than the expected voltage droop due to the ESR and capacitor discharge etc.
- (e) The LED labeled "3.3 Volts" should now be ON and the LED labeled "Power Good" should also be ON. If "Power Good" is not ON, then turn "PGOOD Reference" R₁₅ anticlockwise slowly until the "Power Good" LED is ON.

- (f) Connect a voltmeter across the supercapacitor, which is also across R_L and "CON_CAPXX" (V_{R_L}). Slowly reduce the power supply voltage and note V_{R_L} when the "Power Good" LED turns OFF. Slowly increase the power supply voltage and note V_{R_L} when the "Power Good" LED turns ON. The difference between the two readings is the hysteresis voltage width V_w.
- (g) Adjust "PGOOD Feedback" R_{23} (anti-clockwise increases V_w) and repeat (e)&(f) until the desired hysteresis width is achieved.
- 6.3 Adjusting the High Threshold with "PGOOD Reference" R₁₅
 - (a) Turn "PGOOD Reference" R15 fully clockwise and then reduce the power supply voltage until the "Power Good" LED is OFF.
 - (b) Adjust the power supply voltage so $\,V_{R_{\rm L}}$ equals the desired V_TH. Turn "PGOOD Reference" R15 slowly anti-clockwise until the "Power Good" LED turns ON.
 - (c) Check that the "Power Good" LED turns ON and OFF at the desired levels. This can be done by varying the power supply voltage in both directions so that $V_{R_{\rm r}}$ is less than $V_{\rm TL}$ and then greater than $V_{\rm TH}$.

(d) Remove R_L.

6.4 Replacing the Potentiometers with Fixed Resistors

The potentiometers on the Evaluation Board are included to provide flexibility in evaluating many different applications. In a final design for production the resistance of the potentiometers would have been decided and therefore they can be replaced with fixed resistors. This section includes the equations that can be used to theoretically determine the value of these resistors. The value of these resistors can also be found practically by measuring the resistance of the potentiometers out of circuit once the circuit has been successfully adjusted as above.

$$R22 + R23 = \frac{55k}{V_{W}}$$
(4)

$$R15 + R16 = \frac{4k7V_{TH}}{5 + V_W - V_{TH}}$$
(5)

$$R2 = \frac{22k}{\frac{56}{I_{L}} - 1}$$
(6)

6.5 Limits of Adjustment

From the schematic in the Appendix it can be seen that;

	R22=47k Ω R23=500k Ω potentiometer R15=50k Ω potentiometer R16=3k9 Ω R2= 2k Ω potentiometer
From equation 4;	$0.1V \le V_W \le 1.2V$
From equation 5;	0.1 V = V W = 1.2 V
. ,	$2.3V \le V_{TH} \le 4.7V$ (V _W =0.1V)
	$2.4V \le V_{TH} \le 4.9V (V_W = 0.3V)$
	$2.8V \le V_{TH} \le 5.7V (V_W = 1.2V)$
From equation 6;	
	$0A \le I_L \le 4.7A$

If these limits do not suit the application then resistors can be replaced on the Evaluation Board according to equations 4,5 and 6.

7.0 Connecting the Evaluation Board

The evaluation board is inserted into the Host and the CF Card under test is inserted into the Evaluation Board, as shown in figure 2. The supercapacitor terminals are joined to the connector labeled "CON_CAPXX". The terminals of "CON_CAPXX" are labeled "GND_OUT" and "VCC_OUT". These are to be connected as close as possible to the ground and positive supply of the Pulsed Load respectively. There are many power architectures where the supercapacitor may be placed. For example, the Pulsed Load may be a GPRS module or a DC/DC converter. For the least voltage droop (and maximum benefit from the supercapacitor's low ESR) it is important to minimise the resistance between the supercapacitor and its load. Therefore the wires from "CON_CAPXX" to the Pulsed Load should be as short and as thick as practical.

Warning: As stated in section 2.0, if V_{CC} is chosen to be 5V then the voltage at the supercapacitor must be dropped to < 4.5V by including a series diode. The diode (D10) was chosen such that the minimum load current (quiescent current) gives an acceptable voltage drop. The minimum load can be increased by reducing the supercapacitor balancing resistors (R5 & R6). The CF specification states that the 5V rail is \pm 10% and therefore (in theory) the rail may be as high as 5.5V. In this rare case a voltage drop of 1V is required. If D10 does not give enough voltage drop for the minimum current case then two diodes in series may be needed. Alternatively a diode with different characteristics can be substituted.

Note: The number 1 pin of a header or jumper has a small triangle pointing to it.

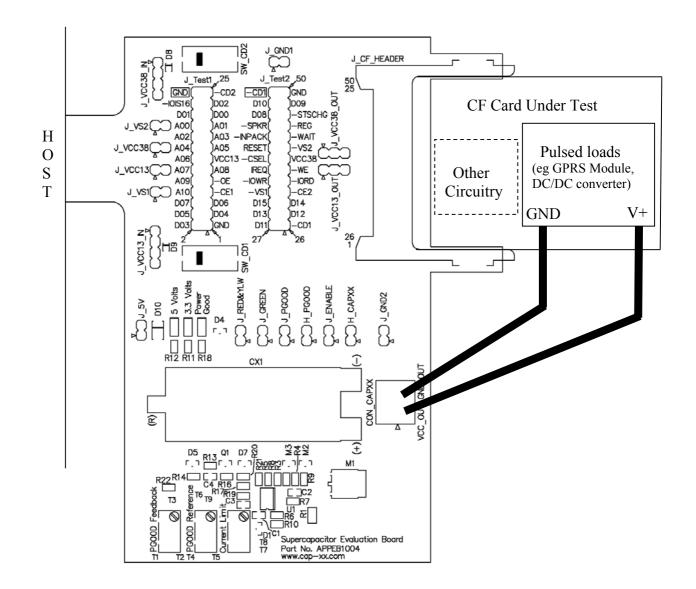


Figure 2 Typical connection of Evaluation Board

7.1 V_{CC} Modes

Figure 2 shows the typical way for connecting the Evaluation Board. V_{CC} on the CF Card Under Test is generally supplied by one of two modes. Mode 1, being the most common, is when V_{CC} is supplied directly from the host (via "J_CF_HEADER" pins 13 and 38). These V_{CC} rails supply all the circuitry on the CF Card Under Test ("Other Circuitry") except for the "Pulsed loads (V+)", which is supplied by the supercapacitor with the external wires. In this mode V_{CC} is available to the "Other Circuitry" as soon as the CF Card Under Test is powered up, whereas the supercapacitor supply to the "Pulsed loads" is delayed by the charge up time of the supercapacitor according to equation 1.

Connections common to both Mode 1 and 2 are;

- (a) Connect external wires (thick and short) from "CON_CAPXX" to the "Pulsed loads" on the CF Card Under Test.
- (b) Place jumpers on pins 3 and 4 of "J_VCC13_IN" and "J_VCC38_IN". Remember to use the series diode (remove "J_5V") if using the 5V rail.
- (c) Place jumpers on "J_RED&YLW", "J_GREEN", "J_PGOOD" and "J_ENABLE",.
- (d) Remove jumpers on "J_VS1", "J_VS2".

Mode 1 is accomplished by the following;

- (a) Connect jumpers on "J_VCC13" and "J_VCC38".
- (b) Remove jumpers across pins 1-2 of both "JVCC_13_OUT" and "JVCC_38_OUT". Make sure that V_{CC} on the CF card under test is not connected to the Pulsed Load V+. Otherwise V_{CC} will be short circuited by the supercapacitor when it is discharged and the current limit circuit is not in this path.

Mode 2 is when the supercapacitor supplies both the V_{CC} for the PC Card Under Test ("Other Circuitry") as well as the "Pulsed loads". In this mode all supplies are delayed according to equation 1. Any voltage ripple on the supercapacitor due to large currents will appear on the V_{CC} rail.

Mode 2 is accomplished by the following;

- (a) Remove the jumpers on "J_VCC13" and "J_VCC38".
- (b) Either ensure that V_{CC} on the CF card under test is connected to the Pulsed Load V+ and supply the load via thick wires as per Figure 2 or place jumpers across pins 1-2 of both "JVCC_13_OUT" and "JVCC_38_OUT".

There are many other modes available. The Evaluation board is designed for flexibility by allowing each section to be isolated or connected to external circuits.

NOTE: Care must be taken, in which ever mode is chosen, so that the charge up time of the supercapacitor does not affect the operation of any reset or power rail monitoring circuitry etc. As described in section 4.0 and 5.0, the "J_ENABLE" and "H_PGOOD" signals may need to be interfaced with the CF Card Under Test for proper control.

7.2 Current Measurement

Currents can be measured with a current probe or a voltage across a sense resistor. A jumper can be replaced by an external wire loop which the current probe can clamp on. If a current probe is not available then a sense resistor can be used in place of the jumpers. The voltage dropped across the resistor divided by the value of the resistor equals the current.

7.3 Card Detect

The correct insertion of a CF Card is detected when both pins 25 and 26 are grounded. These pins are typically grounded on the CF Card Under Test. However, the ground signal can also be replicated by jumpering –CD1 and –CD2 to ground on "J_Test1" and "J_Test2". The removal and insertion of the card can be simulated by depressing and releasing either of the two micro-switches "SW_CD1" or "SW_CD2".

7.4 Voltage Select

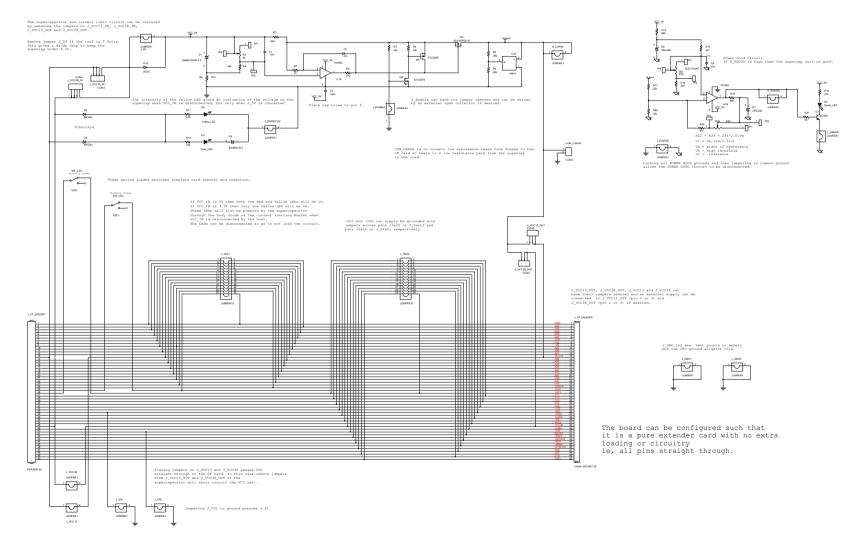
The CF Card Under Test chooses the V_{CC} voltage rail using pin 33 (-VS1). If -VS1 is grounded then a V_{CC} of 3.3V is requested, if it is left floating then 5V is requested. This signal can be replicated with "J_VS1". Placing a jumper on "J_VS1" forces the signal to ground and therefore requests 3.3V. "J_VS2" is undefined and should be left floating.

8.0 Disconnecting Circuits for Reduced Load

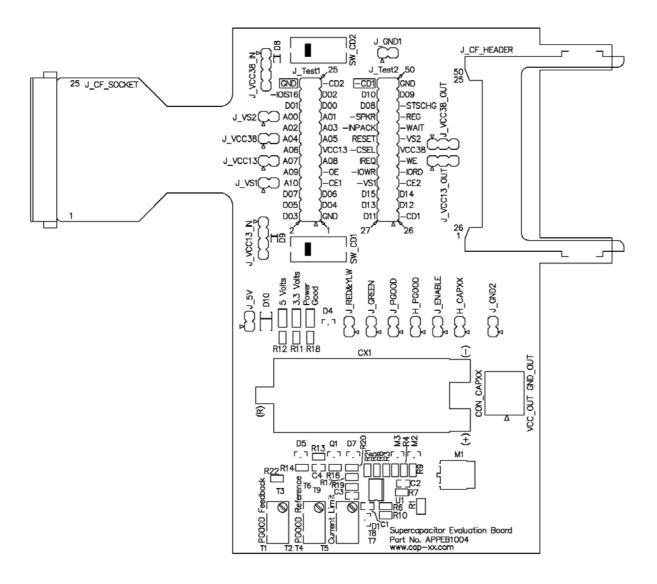
The minimum voltage on some loads may be critical. Any current that the Evaluation Board uses contributes to the droop on the input voltage. If the droop becomes excessive then some of the functions on the Evaluation Board can be disconnected to save current and therefore increase the input voltage. The red and yellow LEDS can be disconnected by removing the jumper "J_RED&YLW". The green LED can be disconnected by removing the jumper "J_GREEN". The entire PGOOD circuit can be disconnected by removing the jumper "J_PGOOD".

Appendix

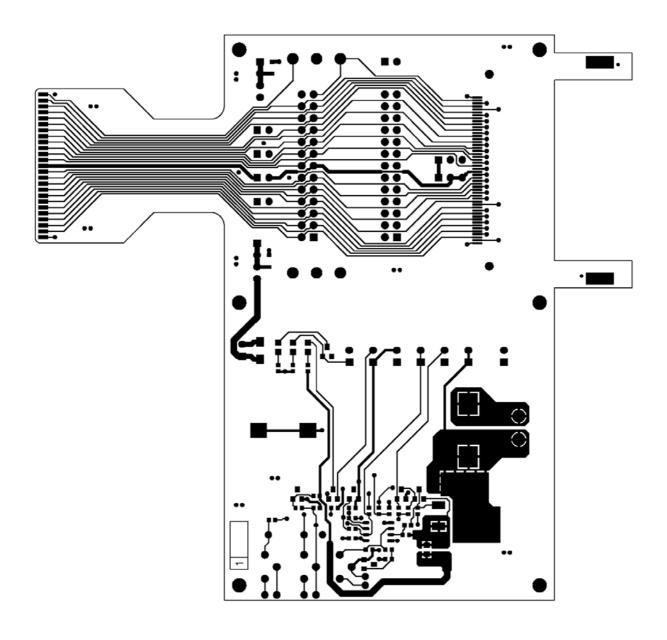
Schematic



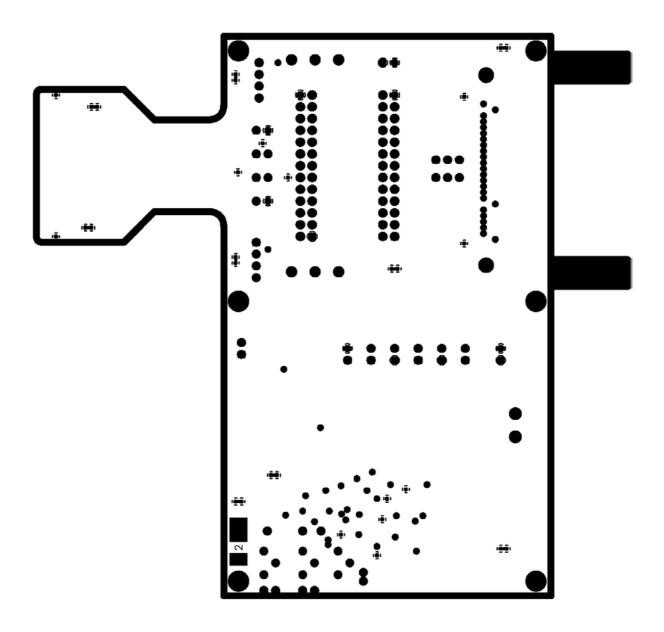
PCB Top Overlay



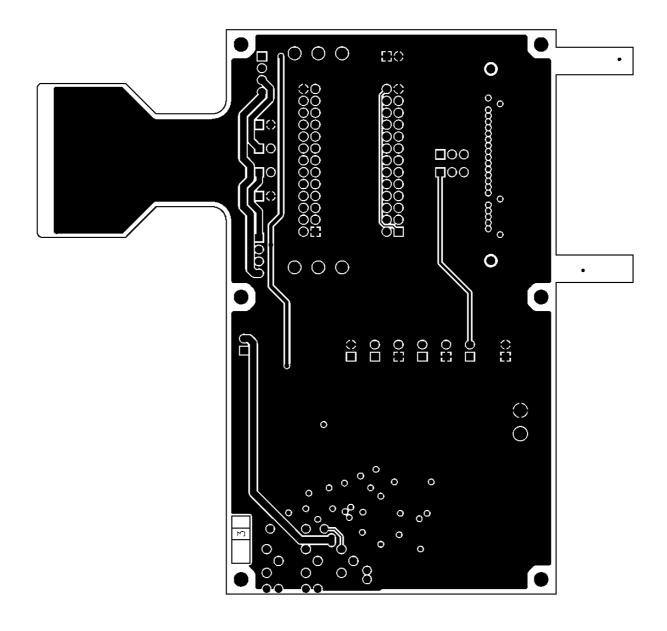
PCB Top Layer



PCB 2nd Layer



PCB 3rd Layer



PCB Bottom Layer

